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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/144,579	08/31/98	TSANG	D 1138-71

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/144,579	Applicant(s) Tsang et al
	Examiner Loke	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 23, 2001* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *43-107* is/are pending in the application.

4a) Of the above, claim(s) *67-97, 99-102, 104, and 105* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *43-66, 98, 103, 106, and 107* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *11*

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

1. Newly submitted claims 67-97, 99-102, 104 and 105 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claims 43-107 are directed to the following patentably distinct species of the claimed invention:

Claims 43-66, 98, 103, 106 and 107 are directed to a recessed gate field effect power MOS device having a vertically oriented channel, classified in class 257, subclass 330.

Claims 67-97, 99-102, 104 and 105 are directed to a vertical double-diffused insulated gate transistor, classified in class 257, subclass 341.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 67-97, 99-102, 104 and 105 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

2. Claims 43-66, 98, 103, 106 and 107 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification discloses a metal silicide layer formed over the doped polysilicon (page 11, line 27 to page 12, line 1). The specification never discloses a gate metal layer coextending over the doped polysilicon as claimed in claim 43.

The specification never discloses an upper metal layer contacting the gate conductor through a via in the insulating layer as claimed in claim 44.

The specification never discloses a portion of the upper metal layer over the insulative layer contacts the source conductor in electrical isolation from the gate conductor as claimed in claim 45.

The specification never discloses an upper metal layer over the insulating layer and contacting the vertically-extending source conductor through a via in the insulating layer as claimed in claim 46.

The specification never discloses the claimed subject matters as claimed in claims 60-65.

The specification never discloses the insulating layer comprises at least one of the group consisting of oxide, nitride, glass and phosphosilicate glass (PSG) as claimed in claim 66.

The specification never discloses a metal disposed coextensively over the doped polysilicon in the conductive gate structure as claimed in claim 98.

The specification never discloses the metallization contacting the gate structure through the insulating layer as claimed in claim 98.

The specification never discloses the metallization over the insulating layer comprises aluminum as claimed in claim 103.

3. Claims 45, 51, 52, 55, 56, 65 and 66 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 45, line 2, "the insulative layer" has no antecedent basis.

In claim 51, line 2, "one of said vertically-oriented layer" is unclear because claim 43 only discloses one vertically-oriented layer.

In claim 51, lines 2-3, "one of said vertically-oriented sidewall spacer" is unclear because claim 50 only discloses one vertically-oriented sidewall spacer.

In claim 52, line 2, "the sidewall spacers" has no antecedent basis.

In claim 55, line 4, "said plurality" is unclear whether it is being referred to "said plurality of islands".

In claim 56, line 5, "the fingers of said plurality" is unclear whether it is being referred to "said plurality of said finger".

In claim 65, line 2, "the upper metal layer" has no antecedent basis.

In claim 66, line 2, "the insulating layer" has no antecedent basis.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 43-48, 50-53, 57, 58, 60-66, 98, 103 and 106 insofar, as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Korman et al. (PTO-1449 filed on 5/23/01)

In regards to claims 43 and 98, Sakamoto discloses a transistor in fig. 4(d). It comprises: a gate trench formed on a drain substrate [1,3]; p-type body region [11] and vertical channel and source regions [11, 12] formed between the trenches; insulating layer [4, 9] formed adjacent to the gate electrode [8]; the vertically-insulative layers [4] being formed by a deposited film of uniform lateral thickness and the laterally-extending insulative layer [9] being separately formed of a deposited isolation material; a metal source electrode [15] formed on the regions [11, 12, 9].

Sakamoto differs from the claimed invention by not having a gate metal layer coextending over the doped polysilicon of a gate conductor.

Korman et al. shows a metal silicide (titanium silicide) layer [156] formed on the polysilicon gate conductor [132] in a vertical MOSFET in fig. 1.

Since both Sakamoto and Korman et al. teach a polysilicon gate electrode in a vertical MOSFET, it would have been obvious to have the metal silicide layer of Korman et al. in Sakamoto because it reduces the resistance of the gate electrode.

It would have been obvious to have the oxide layer as the gate insulating layer because it is a conventional gate insulating material.

In regards to claim 47, fig. 4(d) of Sakamoto differs from the claimed invention by not showing the first vertical layer portion has a lateral thickness less than a vertical height thereof.

Fig. 3 of Sakamoto shows the first vertical layer portion [11] has a lateral thickness than a vertical height thereof.

Since both figs. 4(d) and 3 of Sakamoto teach a source electrode formed in a trench in a vertical MOSFET, it would have been obvious to have the p-type base region of fig. 3 of Sakamoto in fig. 4(d) of Sakamoto because it reduces the resistance of the base region.

In regards to claim 48, it would have been obvious for the first vertical layer portion has a lateral thickness less than 1 micron because it depends on the size of the transistor cell and the packing density of the transistor cells.

In regards to claim 58, fig. 4(d) of Sakamoto differs from the claimed invention by not showing a base region made of p-type layer.

Fig. 7 of Sakamoto shows a p-type layer [1'] formed under the n-type layer [2, 3].

Since figs. 4(d) and 7 of Sakamoto show a vertical transistor, it would have been obvious to have the p-type layer of fig. 7 of Sakamoto in fig. 4(d) of Sakamoto because it can form a pnpn type transistor.

In regards to claims 60, 64, it would have been obvious for the gate metal layer comprises aluminum because it is a conventional gate electrode material.

In regards to claim 65, it would have been obvious for the upper metal layer comprises aluminum because it is a conventional source electrode material.

In regards to claims 61, 63, it would have been obvious for the gate metal layer comprises plateable metal because it is a conventional gate electrode material.

In regards to claim 62, it would have been obvious for the gate conductor comprises a refractory metal silicide over the doped polysilicon, and beneath the gate metal layer because it lowers the resistance of the gate electrode.

In regards to claim 103, it would have been obvious for the metallization over the insulating layer comprises aluminum because it is a conventional source electrode material.

6. Claims 49 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Korman et al., further in view of Davies.

Sakamoto differs from the claimed invention by not showing a p+ type body region.

Davies shows a p+ type body region [21] formed in a p-type base region [17] in a vertical MOSFET in fig. 1.

Since both Sakamoto and Davies teach a vertical MOSFET, it would have been obvious to have the p+ type body region of Davies in Sakamoto because it prevents parasitic bipolar transistor turn on and it extends the safe operating area of the transistor.

7. Claims 55, 56, 59 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Korman et al., further in view Blanchard.

In regards to claims 55, 107, Sakamoto differs from the claimed invention by not showing each of the plurality of cells surrounded by the gate trench.

Blanchard shows each of the plurality of cells surrounded by the gate trench in fig. 9a.

Since both Sakamoto and Blanchard teach a vertical MOSFET with a trench gate, it would have been obvious to have the transistor cell structure of Blanchard in Sakamoto because it is a widely used transistor cell structure in power MOSFET.

In regards to claim 59, Sakamoto further differs from the claimed invention by not showing a trench gate oxide with two different thickness.

Blanchard shows the gate oxide layer [32] having a thick oxide layer at the bottom of the gate trench and a thin oxide layer at the upper portion of the gate trench in fig. 3.

Since both Sakamoto and Blanchard teach a vertical MOSFET with a trench gate, it would have been obvious to have the gate oxide layer of Blanchard in Sakamoto because it increases the breakdown voltage of the device.

In regards to claim 56, Sakamoto differs from the claimed invention by not showing the gate structure configured as a finger.

Blanchard shows the gate structure configured as a finger in fig. 9b.

Since both Sakamoto and Blanchard teach a vertical MOSFET with a trench gate, it would have been obvious to have the gate structure of Blanchard in Sakamoto because it is a widely used gate structure in power MOSFET.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920.

sl

August 5, 2001

Steven Loke
Primary Examiner